

Catalog of Products

2007

*Customer-driven solutions for all your
data transfer needs.*



Engineering Design Team



מיליטרם

הקבוצה מספר 1
במחשבים עבור פרוייקטים
בתצורות:

PC104

PC104+

cPCI

cPCI Express

VME

PCI

ומחשבים ניידים



Telecommunications | Telemetry

High-speed input/output interfaces support a wide variety of protocols and signal levels, including LVDS, RS422, ECL, and PECL, and single- and multiple-channel, serial or parallel data transfers.

Main Boards

- | | |
|-----------|---|
| 04 | PCI SS
<i>Upgraded version of the PCI SS with more memory and a larger, robust FPGA with processing capabilities.</i> |
| 05 | PCI GS
<i>Provides a high-speed 16-channel DMA controller and a large field-programmable gate array and memory for flexible application programming. Intended to be used with one of a variety of mezzanine boards.</i> |

Mezzanine Boards

- | | |
|-----------|--|
| 06 | PCI GS OC192
<i>Bidirectional optical carrier interface supporting synchronous optical network (SONET) OC-192, synchronous data hierarchy (SDH) STM-64 telecommunications standards, and 10 GB Ethernet on one port; on the second port, supports OC-3/STM-1, OC-12/STM-4, OC-48/STM-16, and 1 GB Ethernet.</i> |
| 07 | PCI SS/GS OCM
<i>Synchronous optical network (SONET) OC-3, OC-12, OC-48 and synchronous data hierarchy (SDH) STM-1, STM-4, STM-16 or 10 GB Ethernet telecommunications board.</i> |
| 08 | PCI SS/GS HRC
<i>Used for satellite data acquisition and communications network monitoring; 75-ohm BNC or LC fiber-optic extension connectors.</i> |
| 09 | PCI SS/GS 16TE3
<i>Provides 16 T3 or E3 channels for user-defined telecommunications switching or monitoring applications.</i> |
| 10 | PCI SS/GS Combo 3
<i>Used for satellite data acquisition and telecommunication network monitoring. Uses ECL signal levels with register-selectable input-output on differential connector pins. Choose ECL, LVDS, or RS422 signal levels. Has 4 E3/T3 and 16 E1/T1 channels.</i> |
| 11 | PCI SS/GS SRXL
<i>Satellite telemetry receiver with Gray chips; provides software-defined radio functionality. Allows simultaneous input of IF and L-Band signals, down converts to baseband of I and Q data. A 12-bit A-D conversion sent to the on-board FPGA gives the option of eight channels of digital down conversion.</i> |
| 12 | PCI SS/GS SSE
<i>Synchronous serial interface (400 MB per second) for telemetry, satellite, and monitoring applications.</i> |
| 13 | PCI SS/GS ECL
<i>Provides 32 differential ECL inputs or outputs for telemetry, satellite, and monitoring applications.</i> |
| 14 | PCI SS/GS LVDS/RS422
<i>Provides 33 differential LVDS or RS422 signals, inputs or outputs in groups of four (2 channels).</i> |

Digital Video

EDT manufactures a broad line of industrial digital interface, supporting RS422, LVDS, and Camera Link digital image output formats.

- | | |
|-----------|---|
| 15 | RCX LVDS/RS422
<i>Converts LVDS or RS422 signals from most digital cameras to fiber-optic cable.</i> |
| 16 | RCX C-Link
<i>Fiber-optic adapter for Camera-Link™ cameras; distances up to 10 km possible.</i> |
| 18 | PCI DV FOX + RCX/RCX C-Link
<i>PCI fiber-optic interface for use with RCX C-Link and RCX LVDS/RS422.</i> |
| 20 | PCI DV C-Link
<i>Provides high-resolution image capture for Camera Link monochrome and color digital cameras.</i> |
| 21 | PCI DVa
<i>CCD and CMOS camera interface provides high-speed image capture for RS422 or LVDS devices.</i> |
| 22 | PMC DV C-Link
<i>Like the PCI DV C-Link, but in the PMC form factor.</i> |
| 23 | cPCI DV C-Link
<i>Like the PCI DV C-Link, but in the compact PCI form factor.</i> |
| 24 | PCI DV CLS
<i>Simulator that generates Camera Link camera data.</i> |

General Purpose | Military

EDT's general-purpose data acquisition board uses RS422 or LVDS signal levels while our 1553 interface provides connectivity between MIL-STD 1553 avionics bus devices and PCI local bus computers.

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| 25 | PCI CDa
<i>High-speed (up to 200 MB/second continuously) general-purpose parallel and synchronous serial data input/output interface. RS422 or LVDS signal levels.</i> |
| 26 | PCI 53B
<i>PCI bus to MIL-STD 1553B serial interface. Supports bus controller, bus monitor and 31 remote terminals.</i> |



PCI SS Main Board

Description

The PCI interface connects a mezzanine board to the PCI local bus. It provides DMA and target-access resources. The high-speed 16-channel DMA controller allows flexible access to host memory. A large user-programmable Xilinx and memory allow flexible application data processing.

A PCI SS/GS Bridge is available to connect two PCI SS boards.

Specifications

PCI Local Bus Compliance	PCI Version Data Width Number of Slots Transfer Size DMA (Direct Memory Access) PCI Local Bus Memory Space Clock Rate	PCI 2.2 32 bits 1 Up to 1024 bytes per transfer Yes Approximately 66 KB 33 MHz or 66 MHz
External Connectors	Five CMC-style (IEEE 1386) mezzanine connectors One 40-pin ATA-style connector with 30 low-voltage TTL signals for external boards or user interface Xilinx debug One 8-pin .100" x 8 row square .025" square pins for six external debug LEDs	
User Interface Xilinx	XCV1000E or optional XCV600E or XCV2000E	
Static Local Memory	Standard: Two banks of 256K x 36-bit word (1 MB) Optional: Two banks of 512K x 36-bit word (2 MB), two banks of 1M x 36-bit word (4 MB), no RAM HRC and OCM: one bank of 256K, one bank of 512K, or one bank of 1M	
Clock Generators	Four programmable independent phase-locked loop clock generators Reference clock may be selected as 10.3681 MHz, 40 MHz, or PCI clock An infinite number of frequencies is possible. The telecommunications industry standards 1.544 MHz, 2.048 MHz, 6.312 MHz, 8.448 MHz, 34.368 MHz, and 44.736 MHz can be set with less than +/-50 ppm error.	
Physical	Number of Slots Dimensions	1 4.2" x 6.6"
Environmental	Temperature Humidity	Operating: 0° to 40°C Non-operating: -40° to 70°C Operating: 1% to 90% non-condensing @ 40°C Non-operating: 95% non-condensing @ 45°C
Mezzanine Board Features	From 3.875" x 6" up to 3.875" x 12.283" Typical .250" component height facing PCI SS main board .070" component height opposite side .500" component height if mezzanine extends past PCI SS main board Mating connector CMC-style (IEEE 1386), AMP p/n 120527-1, or Molex p/n 71436-2164 221 low-voltage TTL I/O signals	
Available EDT Mezzanine Boards and Signals	Combo: 16 E1/T1, 4 E3/T3, 16 ECL I/O Combo 2: 16 E1/T1, 4 E3/T3, 16 LVDS or RS-422 I/O Combo 3: Same I/O as Combo, but with electronic direction control on telecom interfaces LVDS: 32 LVDS I/O RS422: 32 RS-422 I/O ECL: 32 ECL I/O HRC: 4 E4, OC-3/STM-1 I/O OCM: 2 OC-3/STM-1, OC-12/STM-4, OC-48/STM-16 I/O, 1 Gb Ethernet SRXL: L-Band and IF radio receiver OC192: Same as OCM plus OC192/STM-16 and 10 Gb Ethernet	
40-Pin Expansion Connector	30 low-voltage TTL signals with ATA ground pinout so high-quality/low-cost ATA-100 cables can be used to connect external boards.	

Features

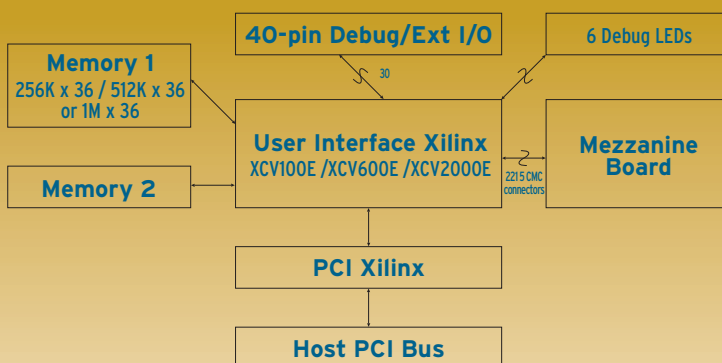
221 low-voltage TTL user-programmable signals connected to mezzanine board

Large user-programmable FPGA, up to Xilinx XCV2000E

Two synchronous static memory banks

16 independent DMA channels to host memory

66 MHz 32-bit PCI for fast transfers



Description

The PCI interface connects a mezzanine board to the PCI local bus. It provides DMA and target-access resources. The high-speed 16-channel DMA controller allows flexible access to host memory. A large user-programmable Xilinx and memory plus on-chip Power PC processors allow flexible application data processing.

A PCI SS/GS Bridge is available to connect two PCI GS boards.



PCI GS Main Board

Specifications

PCI Local Bus Compliance	PCI Version Data Width Number of Slots Transfer Size DMA (Direct Memory Access) PCI Local Bus Memory Space Clock Rate	PCI 2.2 32 bits 1 Up to 1024 bytes per transfer Yes Approximately 1 KB 33 MHz or 66 MHz
External Connectors	Five CMC-style (IEEE 1386) mezzanine connectors One 40-pin ATA-style connector with 30 low-voltage TTL signals for external boards or user interface Xilinx debug. Eight signals may be used for Xilinx gigabit serial I/O (Rocket™ I/O). One 8-pin .100" x 8 row square .025" square pins for six external debug LEDs	
User Interface Xilinx	XC2VP50 or optional XC2VP70	
Static Local Memory	1M x 36-bit word (4 MB) or optional 2M x 36-bit word (8 MB) synchronous static RAM	
Dynamic Memory	200-pin SODIMM socket for optional DDR memory module. Up to 1 gigabyte.	
Clock Generators	Four programmable independent phase-locked loop clock generators. Reference clock may be selected as 10.3681 MHz, 40 MHz, or PCI clock. An infinite number of frequencies is possible. The telecommunications industry standards 1.544 MHz, 2.048 MHz, 6.312 MHz, 8.448 MHz, 34.368 MHz, and 44.736 MHz can be set with less than +/-50 ppm error.	
Physical	Number of Slots Dimensions	1 4.2" x 6.6"
Environmental	Temperature Humidity	Operating: 0° to 40°C Non-operating: -40° to 70°C Operating: 1% to 90% non-condensing @ 40°C Non-operating: 95% non-condensing @ 45°C
Mezzanine Board Features	From 3.875" x 6" up to 3.875" x 12.283" Typical .250" component height facing PCI GS main board .070" component height opposite side .500" component height if mezzanine extends past PCI GS main board Mating connector CMC-style (IEEE 1386), AMP p/n 120527-1, or Molex p/n 71436-2164 221 low-voltage TTL I/O signals	
Available EDT Mezzanine Boards and Signals	Combo: 16 E1/T1, 4 E3/T3, 16 ECL I/O Combo 2: 16 E1/T1, 4 E3/T3, 16 LVDS or RS-422 I/O Combo 3: Same I/O as Combo, but with electronic direction control on telecom interfaces LVDS: 32 LVDS I/O RS-422: 32 RS-422 I/O ECL: 32 ECL I/O HRC: 4 E4, OC-3/STM-1 I/O OCM: 2 OC-3/STM-1, OC-12/STM-4, OC-48/STM-16 I/O, 1 Gb Ethernet SRXL: L-Band and IF radio receiver OC192: Same as OCM plus OC192/STM-16 and 10 Gb Ethernet	
40-Pin Expansion Connector	30 low-voltage TTL signals with ATA ground pinout so high-quality/low-cost ATA-100 cables can be used to connect external boards. Eight signals may be used for Xilinx gigabit serial interfaces (Rocket™ I/O).	

Features

221 low-voltage TTL user-programmable signals connected to mezzanine board

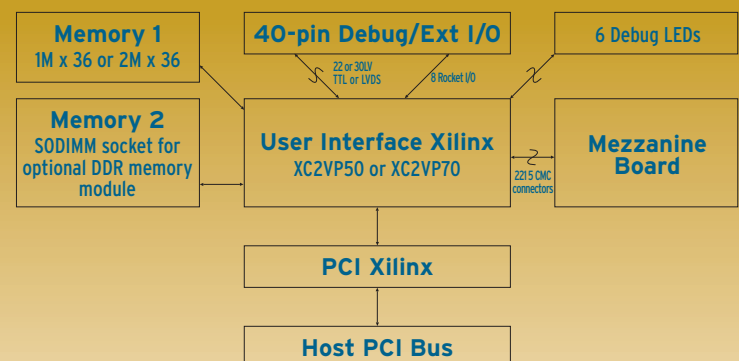
Large Xilinx Virtex™-II Pro FPGA with two power PC processors

Up to 8 megabytes synchronous static memory

Up to 1 gigabyte double data rate (DDR) 200-pin SODIMM socket

16 independent DMA channels to host memory

66 MHz 32-bit PCI for fast transfers





PCI GS OC192

Description

The PCI GS OC192 supports synchronous optical network (SONET) OC192, synchronous data hierarchy (SDH) STM-64 telecommunications standards, and 10 Gb Ethernet. The mezzanine board has one XFP fiber optic LC connector and a second optional SFP fiber optic LC connector.

EDT provides FPGA configuration files that support a variety of protocols, including raw data, framed data, framed and descrambled data, header data, and payload data

Specifications

PCI Local Bus Compliance	PCI Version Data Width Number of Slots Transfer Size DMA (Direct Memory Access) PCI Local Bus Memory Space Clock Rate	PCI 2.2 32 bits 1 Up to 256 bytes per transfer Yes Approximately 66 KB 33 MHz or 66 MHz	
Interface Data Transfer	SONET OC-192 SDH STM-64		
SONET/SDH Protocols	STM-1, -4, -16, -64: concatenated payload Other payloads available upon request		
Ethernet Protocols	IEEE802.3, packet over SONET Header-only or header and payload available upon request		
Optical Characteristics	850 nm Output power Center wavelength Sensitivity Max. input power	OC-3 to OC-48 -9 to -2.5 dBm 830 to 860 nm -20 dBm 0 dBm	OC-192 -3 to -1 dBm 850 nm -7.5 dBm -1 dBm
	1310 nm Output power Center wavelength Sensitivity Max. input power	-10 to -3 dBm 1270 to 1360 nm -18 dBm 0 dBm	-6 to -1 dBm 1290 to 1330 nm -13 dBm -0.5 dBm
	1550 nm Output power Center wavelength Sensitivity Max. input power	-2 to 3 dBm 1500 to 1580 nm -28 dBm -9 dBm	-1 to 2 dBm 1550 nm -15 dBm -1 dBm
User Interface Xilinx	XC2VP50 or optional XC2VP70		
Local Memory	Optional 4 GB RAM is necessary to collect raw data snapshots at rates faster than 1.8 Gb. Faster data rates exceed the continuous transfer rates of PCI SS and PCI GS boards.		
Environmental	Temperature	Operating: 0° to 50°C Non-operating: -40° to 70°C	
	Humidity	Operating: 1% to 90% non-condensing @ 40°C Non-operating: 95% non-condensing @ 45°C	
Physical	Dimensions	4.2" x 5.78" x 0/5"	
	Weight	6/5 oz. typical	

Features

One bidirectional optical carrier interface, SONET OC-192/SDH STM-64 (9953.28 megabits per second), 10 Gb Ethernet, or ITU frequencies available.

Optional second bidirectional multi-rate optical carrier interface, either SONET OC-3/SDH STM-1 (155.52 Mb/sec), OC-12/STM-4 (622.08 Mb/sec), OC-48/STM-16 (2488.32 Mb/sec); 1000 Base-T Ethernet available

Occupies a single PCI local bus slot

PCI GS main board FPGA options: Xilinx XC2VP50 or XC2VP70

Optional 4 GB RAM on the OC-192 mezzanine board

Optional 1 GB RAM on the PCI GS main board

High-speed DMA channel between interfaces and PCI local bus computer

Compatible with PCI platforms running the Solaris™, Windows NT® and Windows® 2000/XP, or Linux

Choose 850 nm, 1310 nm, or 1550 nm transceivers

Description

The PCI SS/GS OCM supports synchronous optical network (SONET) OC-3, OC-12, OC-48 and synchronous data hierarchy (SDH) STM-1, STM-4, STM-16 telecommunications standards. The mezzanine board has two fiber optic LC connectors. One fiber optic connector will support the OC-3/STM-1, OC-12/STM-4, or OC-48/STM-16 standard bit rates, while the other fiber optic connector will support the OC-3/STM-1 or OC-12/STM-4 only. Either fiber optic connector can support a 1000 Base-T copper Ethernet adapter.

EDT provides an FPGA configuration file that makes it possible to output and acquire raw data, detect to a SONET/SDH frame, and descramble a framed signal.



PCI SS / GS OCM

Specifications

PCI Local Bus Compliance	PCI Version	PCI 2.2	
	Data Width	32 bits	
Interface Data Transfer	Number of Slots	1	
	Transfer Size	Up to 256 bytes per transfer	
	DMA (Direct Memory Access)	Yes	
	PCI Local Bus Memory Space	Approximately 66 KByte	
	Clock Rate	33 MHz or 66 MHz	
	SONET OC-3, OC-12, OC-48 SDH STM-1, STM-4, STM-16 Ethernet: 1000 Base-T		
Optical Transmitter	Output power (average)	OC-3, OC-12, OC-48 Connector -10 to -3 dBm	OC-3, OC-12 Connector -15 to -8 dBm
	Center wavelength	1260 to 1360 nm 1300 nm	1300 nm
Optical Receiver	Sensitivity (average power)	-22 to -20 dBm (OC-48) -24 to -20 dBm (OC-12) -25 to -20 dBm (OC-3)	-30 to -28 dBm (OC-12) -31 to -28 dBm (OC-3)
	Saturation (average power)	0 minimum	-8 dBm
	Local Memory	Optional 2 GB RAM that is necessary to collect raw data snapshots at OC-48/STM-16 data rates. These data rates exceed the continuous transfer rates of PCI SS and PCI GS boards.	
Power	1.8 A @ 3.3 V		
Environmental	Temperature	Operating: 0° to 50°C Non-operating: -40° to 70°C	
	Humidity	Operating: 1% to 90% non-condensing @ 40°C Non-operating: 95% non-condensing @ 45°C	
Physical	Dimensions	4.2" x 5.78" x 0.5"	
	Weight	3/5 oz. typical	

Features

Single PCI local bus slot

One bidirectional multi-rate interface, either SONET OC-3/SDH STM-1 (155.52 Mb/sec), OC-12/STM-4 (622.08 Mb/sec), OC-48/STM-16 (2488.32 Mb/sec), or 10 Gb Ethernet

One bidirectional multi-rate interface for SONET OC-3/SDH STM-1, OC-12/STM-4, or 1000 Base-T Ethernet

User-programmable FPGA up to Xilinx XCV2000E (PCI SS) or XC2VP70 (PCI GS)

Optional 2 gigabyte RAM on the OCM mezzanine board

Local memory up to 1 gigabyte (PCI GS)

High-speed DMA channel between interfaces and PCI local bus computer.



PCI SS/GS HRC

Description

The PCI SS HRC and PGI GS HRC boards support STM-1, STS-3, OC-3, and E4 telecommunications standards in various combinations depending on the options. The boards have four connector locations, and each location can be either a 75 ohm BNC coaxial interface with CMI-coded transmission or an LC fiber optic connector. The fiber optic connector is a single-mode 1300 nm transceiver. The coaxial connectors can be set as either input or output by programmable control. Depending on what options are ordered, the connector slot is filled with a fiber optic connector or a coaxial connector. If bidirectional coaxial operation is required, a maximum of two channels will be usable.

EDT configuration files can support framing and descrambling for OC-3/STM-1 framed data.

Specifications

PCI Local Bus Compliance	PCI Version Data Width Number of Slots Transfer Size DVMA Master PCI Local Bus Memory Space Clock Rate	PCI 2.2 32 bits 1 64 bytes per transfer max. Yes Approximately 66 KByte 33 MHz or 66 MHz
Interface Data Transfer	CMI-coded coaxial NRZ fiber optic	
Optical Transmitter	Output power (average) -15.0 to -8.0 dBm Center wavelength 1260 to 1360 nm	
Optical Receiver	Sensitivity (average power) max. -29.0 dBm Saturation (average power) min. -.80 dBm	
Electrical Transmitter Receiver	G.703 standard	
External Connectors	75 ohm BNC or LC fiber optic	
Power	5 V at 1.5 A	
Environmental	Temperature Humidity	Operating: 0° to 50°C Non-operating: -40° to 70°C Operating: 1% to 90% non-condensing @ 40°C Non-operating: 95% non-condensing @ 45°C
Physical	Dimensions Weight	4.2" x 5.78" x 0.5" 3.5 oz. typical

Features

Single PCI local bus slot

Up to four 139.264 Mbit/s E4 or 155.52 Mbit/s serial interfaces useful for OC-3, STS-3, and STM-1

Each interface may be configured as a uni-directional CMI-coded G.703 BNC or a bidirectional 1300 nm single-mode small form factor (SFF) LC fiber optic

Local memory up to 1 gigabyte (PCI GS)

User-programmable FPGA up to Xilinx XCV2000E (PCI SS) or XC2VP70 (PCI GS)

High-speed DMA channel between interfaces and PCI local bus computer

Description

The PCI SS/GS 16TE3 is a mezzanine board with 16 T3 or E3 telecommunication interfaces that can be used for complex, user-defined telecommunications applications. A large Xilinx Virtex™-E (PCI SS) or Virtex™-II Pro (PCI GS)FPGA and associated memory allow the user to process a large amount of telecommunications serial. The high-speed 16-channel DMA controller allows flexible access to host memory.



PCI SS / GS 16TE3

Specifications

PCI Local Bus Compliance (when mounted on PCI SS/GS Main Board)	PCI Version Data Width Number of Slots Transfer Size DMA (Direct Memory Access) PCI Local Bus Memory Space Clock Rate	PCI 2.2 32 bits 1 Up to 256 bytes per transfer Yes Approximately 1 KB 33 MHz or 66 MHz
External Connectors	High-density 62-pin AMP™ receptacle (part number 748394-5) AMP mating connector not included (part number 748367-1)	
E3/T3	Transformer coupled 16 independent E3/T3 interfaces (G.703 compatible) Full duplex signals available on all 16 channels 75 ohm coaxial cable over 1100 feet at speeds up to 51.84 megabytes per second Compliant with ANSI T1.102-1993, Telcordia GR-499-CORE and G.823 for jitter tolerance B3ZS or HDB3 encoder/decoder Select jitter attenuation on transmit or receive	
Physical	Number of Slots Dimensions	1 4.2" x 6.6"
Environmental	Temperature Humidity	Operating: 0° to 40°C Non-operating: -40° to 70°C Operating: 1% to 90% non-condensing @ 40°C Non-operating: 95% non-condensing @ 45°C
Power	PCI SS:2.5 A @ 5 V PCI GS:1.8 A @ 3.3 V	

Features

16 E3/T3 full duplex line interfaces

User-programmable FPGA up to Xilinx XCV2000E (PCI SS) or XC2VP70 (PCI GS)

Local memory up to 1 gigabyte (PCI GS)

16 independent DMA channels to host memory

Fast transfers using a 66 MHz 32-bit PCI



PCI SS/GS Combo 3

Description

The PCI SS/GS Combo 3 is a mezzanine board with multiple telecommunication and ECL interfaces that can be used for complex, user-defined telecommunications applications. A large Xilinx Virtex™-E (PCI SS) or Virtex™-II Pro (PCI GS) FPGA and associated memory allow the user to process a large amount of telecommunications serial or ECL data. The high-speed 16-channel DMA controller allows flexible access to host memory.

Specifications

PCI Local Bus Compliance (when mounted on PCI SS/GS Main Board)	PCI Version Data Width Number of Slots Transfer Size DMVA Master PCI Bus Memory Space Clock Rate	PCI 2.2 32 bits 1 Up to 256 bytes per transfer Yes Approximately 1 KB 33 MHz or 66 MHz
External Connectors	High-density 68-pin AMP™ connector (part number 787169-7) High-density 15-pin AMP™ receptacle (part number 1-1470250-3)	
ECL	16 differential ECL signals; input or output in groups of four Standard ECL signal levels, terminated through 50 Ω to -2 V	
E3/T3	Transformer coupled Four independent E3/T3 interfaces (G.703 compatible) Input, output, or both on eight differential connector pins 75 ohm coaxial cable over 1100 feet at speeds up to 51.84 megabytes per second Compliant with ANSI T1.102-1993, Telcordia GR-499-CORE and G.823 for jitter tolerance B3ZS or HDB3 encoder/decoder Select jitter attenuation on transmit or receive	
E1/T1	Transformer-coupled 16 independent input/output E1/T1 interfaces (G.703 compatible) Input, output, or both on 16 differential connector pins 1.544 MBpersecond (T1), 2.048 MB persecond (E1) Waveforms meet G.703 and T1.102 specifications Exceeds transmit return loss specification ETSI ETS-300166 Jitter attenuation Transmit return loss exceeds ETSI ETS 300166 HDB3 or B8Zs encoder/decoder Analog/Digital and remote loopback	
Physical	Number of Slots Dimensions	1 4.2" x 6.6"
Environmental	Temperature Humidity	Operating: 0° to 40°C Non-operating: -40° to 70°C Heat Output: TBD Operating: 1% to 90% non-condensing @ 40°C Non-operating: 95% non-condensing @ 45°C
Power	2 amps @ 5V	

Features

Input/Output electronically selected rather than jumpered

16 E1/T1 line interfaces

Four E3/T3 line interfaces

16 ECL differential inputs/outputs

User-programmable FPGA up to Xilinx XCV2000E (PCI SS) or XC2VP70 (PCI GS)

Local memory up to 1 gigabyte (PCI GS)

LVDS external clock that can be used to synchronize output data

16 independent DMA channels to host memory

Fast transfers using a 66 MHz 32-bit PCI

Description

The SRXL mezzanine board provides software-defined radio in a PCI platform. The board is designed to mount to the EDT PCI SS and GS main board and accepts simultaneous RF inputs in the L-Band range of 925 to 2175 MHz and the IF ranges from 65 to 225 MHz. Each RF input is processed with a tunable quadrature down converter. The resulting base-band I and Q signals are low-pass filtered and digitized with 12-bit precision at programmable sample rates up to 65 MHz.

The resulting four channels of digital sample data are available as inputs to the Xilinx Spartan-3 FPGA. The Spartan-3 is user-programmable to perform signal processing and/or serve as a configurable switch matrix to route data to the main board and up to two four-channel GC4016 digital down converter Graychips.

Additional user-configurable pro-cessing can be performed on the PCI SS or GS main board user interface Xilinx. The main board provides a flexible high-performance 32-bit 66 MHz PCI DMA interface to host-computer memory and applications.

Features

Provides software-defined radio receiver directly into a PCI local bus board

Simultaneous operation of complete L-Band and IF analog quadrature down converters

Programmable IF local oscillator at 1 MHz tuning resolution for frequencies between 65 and 225 MHz

Programmable L-Band local oscillator at 5 MHz tuning resolution for frequencies between 925 and 2175 MHz

12-bit A/D conversion of L-Band and IF quadrature data (65 MHz maximum sample rate)

Programmable DDS-based sample clock with 32-bit tuning resolution

Onboard TCXO 10 MHz reference clock or optional external reference input

User-programmable Xilinx Spartan-3 XC3S1500 FPGA

Two GC4016 Graychips for up to eight channels of DDC

Connects to EDT PCI SS or PCI GS main boards



PCI SS/GS SRXL

Specifications

L-Band Input	Nominal Input Impedance	75 ohms
	Minimum Return Loss	12 dB
	Minimum Usable Signal Level	-72 dBm
	Maximum Usable Signal Level	3 dBm
	Absolute Maximum Signal Level	10 dBm
	RF Gain Control	60 dB min.
	Base Band Gain Control	19 dB min.
L-Band Local Oscillator	Tuning Range	925 to 2175 MHz
	Tuning Step Size	5 MHz
	Phase Noise (measured)	-72 dB at 40 KHz, -50 dB @ 10 KHz
L-Band Local Demodulator	Base Band LP Filter Cutoff	4 to 33 MHz (-3 dB)
	Transition Band	42 dB/octave
	IQ Phase Error	4 degrees max.
	IQ Gain Error	1.2 dB max.
IF Input	Nominal Input Impedance	75 ohms
	Minimum Return Loss	12 dB
	Minimum Usable Signal Level	-76 dBm
	Maximum Usable Signal Level	-19 dBm
	Absolute Maximum Signal Level	10 dBm
	Variable Gain Control Range	43 (min.) to 60 (typical) dB
IF Local Oscillator	Tuning Ranges	63 to 112 MHz, 125 to 225 MHz
	Tuning Step Size	1 MHz
	Phase Noise (measured)	-72 dB @ 40 KHz, -65 dB @ 10 KHz
IF Demodulator	Base Band LP Filter Cutoff	23 MHz
	Transition Band	24 dB/octave
	IQ Phase Error	3 degrees max.
	IQ Gain Error	0.6 dB max.
Internal 10 MHz Reference	Frequency	10 MHz
	Nominal Frequency Tolerance	+/-0.5 ppm @ 25°C
	Frequency Over Temperature	+/-2.5 ppm @ 0° to 75°C
	Adjustment Range	+/-3 ppm
External 10 MHz Reference Input	Nominal Input Impedance	50 ohms
	Minimum Return Loss	12 dB
	Minimum Usable Signal Level	-10 dBm
	Maximum Usable Signal Level	10 dBm
	Absolute Maximum Signal Level	16 dBm including any DC component
A/D Conversion	Resolution	12 bits
A/D Sample Clock	Range	1 to 60 MHz
	DDS Tuning Word	32 bits
	User-Defined Sample Clock	From FPGA pin phase locked to 10 MHz reference
Connectors	F-type 75 ohms	For L-Band input
	SMB 75 ohms	For IF input
	SMB 50 ohms	For optional reference clock



PCI SS/GS SSE

Description

The PCI SS/GS SSE mezzanine board samples the data on the rising edge of the clock and stores it in host memory through the PCI SS/GS DMA.

One 15-pin D connector is provided. Each channel accepts a differential data signal (two wires) and a differential clock (two more wires) at standard ECL signal levels. The output channel has one differential data signal and one differential clock. All input signals are terminated through 50 ohms to -2 volts.

The PCI SS/GS SSE has an additional differential data signal that can be used in applications where notification of a start or an end of a block transfer is necessary.

Specifications

PCI Local Bus Compliance (when mounted on PCI SS/GS Main Board)	PCI Version Data Width Number of Slots Transfer Size DMVA Clock Rate	PCI 2.2s 32 bits 1 Up to 256 bytes per transfer Yes 33 MHz or 66 MHz
Power	2.4 amps @ 5V	
Environmental	Temperature	Operating: 0° to 40°C Non-operating: -40° to 70°C Heat Output: TBD
	Humidity	Operating: 1% to 90% non-condensing @ 40°C Non-operating: 95% non-condensing @ 45°C
Physical	Dimensions Weight	4.2" x 5.78" x 0.5" 3.5 oz. typical
Cables	Custom cables can be provided	
Reed-Solomon Decoder	Frame Synchronizer	32-bit frame sync pattern 32-bit frame sync mask Flexible framing with up to 15 check frames and up to 15 flywheel frames CCSDS Reed-Solomon (255,223) error correction
	Reed-Solomon Error Correction	5-way interleave depth CCSDS Reed-Solomon (255,223) encoding
	Reed-Solomon Encoding	5-way interleave depth Reed-Solomon code other than (255,223)
	Possible Custom Features	Shortened codes using virtual fill Interleave depth other than 5 Randomization/de-randomization Support for other EDT boards

Features

Transfer rates up to 400 megabits per second per channel

Three channels (two input and one input/one output)

One data bit per channel

ECL-compatible driver/receivers

Implements a high-speed DMA channel between an external device and PCI local bus computer

User-programmable FPGA up to Xilinx XCV2000E (PCI SS) or XC2VP70 (PCI GS)

Local memory up to 1 gigabyte (PCI GS)

Single PCI local bus slot

Reed-Solomon encoding/decoding

Two user-defined LEDs

Optional 32 ECL/RS-422/LVDS signals

Description

The ECL mezzanine board provides 32 differential ECL interface signals for either the PCI SS or PCI GS main boards. The ECL signals can be inputs or outputs in groups of four (two channels). The function of each signal is determined by the FPGA configuration file used on the main board.

The ECL mezzanine board is supplied with FPGA configuration files that implement 16 synchronous serial channels. Each channel inputs or outputs a data signal on the edge of the associated clock. The data is stored in or sent from host memory using the PCI DMA. This configuration provides a simple, flexible solution for telemetry, satellite, and monitoring applications.

A large Xilinx Virtex™-E (PCI SS) or Virtex™-II Pro (PCI GS) FPGA and associated memory allow the user to implement an FPGA configuration and process large amounts of serial ECL data. The separate high-speed 16-channel PCI DMA controller allows flexible access to host memory.

Features

32 ECL input/output signals

Transfer rates up to 60 megabits per second per signal

User-programmable FPGA up to Xilinx XCV2000E (PCI SS) or XC2VP70 (PCI GS)

Local memory up to 1 gigabyte (PCI GS)

LVDS external clock that can be used to synchronize the output data

Single short PCI local bus slot

Fast transfers using a 66 MHz 32-bit PCI

Configuration files for 16 synchronous serial channels

Optional two T1/E1 input/output channels

Optional SSE two simultaneous input channels and one output channel (400 megabit per second synchronous serial ECL)



PCI SS/GS ECL

Specifications

PCI Local Bus Compliance (when mounted on PCI SS/GS Main Board)	PCI Version	PCI 2.2
	Data Width	32 bits
	Number of Slots	1
	Transfer Size	Up to 1024 bytes per transfer
	DMA (Direct Memory Access)	Yes
	PCI Local Bus Memory Space	Approximately 66 KB
	Clock Rate	33 MHz or 66 MHz
External Connectors	High-density 68-pin AMP™ connector (part number 787169-7)	
ECL	32 differential ECL signals; input or output in groups of four Standard ECL signal levels, terminated through 50 ohms to -2V	
Physical	Number of Slots	1
	Dimensions	4.2" x 6.6"
Environmental	Temperature	Operating: 0° to 40°C Non-operating: -40° to 70°C
	Humidity	Operating: 1% to 90% non-condensing @ 40°C Non-operating: 95% non-condensing @ 45°C



PCI SS/GS LVDS/RS422

Specifications

PCI Local Bus Compliance (when mounted on PCI SS/GS Main Board)	PCI Version	PCI 2.2
	Data Width	32 bits
	Number of Slots	1
	Transfer Size	Up to 1024 bytes per transfer
	DMA (Direct Memory Access)	Yes
	PCI Local Bus Memory Space	Approximately 66 KB
	Clock Rate	33 MHz or 66 MHz
External Connectors	High-density 68-pin AMP™ connector (part number 787169-7)	
LVDS/RS422	33 differential LVDS signals Standard LVDS or RS-422 signal levels, terminated with 100 ohm line to line	
Physical	Number of Slots	1
	Dimensions	4.2" x 6.6"
Environmental	Temperature	Operating: 0° to 40°C Non-operating: -40° to 70°C
	Humidity	Operating: 1% to 90% non-condensing @ 40°C Non-operating: 95% non-condensing @ 45°C

Description

The LVDS/RS-422 mezzanine board provides 33 differential LVDS or RS-422 signals for either the PCI SS or PCI GS main boards. The LVDS/RS-422 signals can be inputs or outputs in groups of four signals. The function of each signal is determined by the FPGA configuration file programmed on the main board.

The PCI SS/GS LVDS/RS-422 mezzanine board is supplied with FPGA configuration files that implement 16 synchronous serial channels. Each channel inputs or outputs a data signal on the edge of the associated clock. The data is stored in or sent from host memory using the PCI DMA. This configuration provides a simple, flexible solution for telemetry, satellite, and monitoring applications.

A large Xilinx Virtex™-E (PCI SS) or Virtex™-II Pro (PCI GS) FPGA and associated memory allow the user to implement an FPGA configuration and process a large amount of serial data. The separate high-speed 16-channel PCI DMA controller allows flexible access to host memory.

Features

33 LVDS (standard) or RS-422 (optional) input/output signals

Transfer rates up to 90 megabits per second using a single channel; 64 megabits per second using all 16 channels

Provides 16 high-speed DMA channels between LVDS or RS-422 devices and a PCI local bus computer

User-programmable FPGA up to Xilinx XCV2000E (PCI SS) or XC2VP70 (PCI GS)

Local memory up to 1 gigabyte (PCI GS)

Single short PCI local bus slot

Fast transfers using a 66 MHz 32-bit PCI

Configuration file for 16 synchronous serial channels

Description

An EDT RCX module converts the LVDS or RS422 signals from most digital cameras to fiber-optic cable. The EDT RCX module sends the camera data to an EDT PCI DV FOX installed in the host computer.

Alternately, two RCX modules may be used to form a fiber-optic extension cord, with one module at the camera and the other module driving a possibly third-party frame grabber. The following block diagrams show a few of these configurations, other combinations are possible.

The RCX module contains an FPGA that can be updated from the host computer to accommodate new camera types.



RCX LVDS / RS422

Specifications

RCX Module Specifications	Fiber-optic connector type Laser Safety Indicators Dimensions Weight	LC duplex Class 1 Two LEDs that shows the state of the fiber-optic link and onboard electronics 2.7" x 5.6" x 1.3" 10.1 oz.
Environmental	Temperature Humidity	Operating: 0° to 40°C Non-operating: -20° to 60°C (extended temperature available) Operating: 20% to 80% non-condensing @ 40°C Non-operating: 95% non-condensing @ 40°C
Video Interface	The EDT RCX module interfaces to AIA digital cameras of up to 24 data bits through an AMP 787169-7 high-density 68-pin connector using RS422 or LVDS differential signalling.	
Fiber-Optic Cables and Transceivers	Transceivers 850 nm VCSEL transceiver 1300 nm laser transceiver	850 nm or optional 1300nm Fiber type: 62.5/125 millimeter MMF Distance: 300 meters Fiber type: 8/125 millimeter SMF Distance: 10 kilometers Fiber-optic cables are not included
Power Supply	Supply Power	10 to 32V DC, 4 watts maximum. EDT provides an AC mains power supply Connector Switchcraft 712A, center positive. 100 to 240V, 50 to 60 Hz from AC mains, 12V DC out
Physical	Dimensions Weight Power	2.4" x 4.5" x 1.5" 10 oz. 100 to 240V, 50 to 60 Hz from AC mains, 12V DC out
Flash Memory	Can be updated using a program on a host computer operating through an appropriate EDT frame grabber such as the PCI DV FOX.	

Features

Supports 8 to 24 bits per pixel, LVDS or RS422 signalling

Sends data to an EDT PCI DV FOX frame grabber

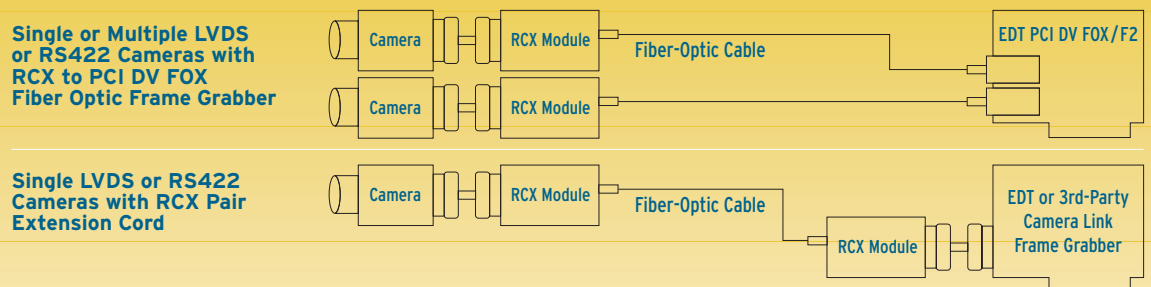
Two EDT RCX modules can be used as a fiber-optic extension cord

68-pin connector provides connection to a wide range of AIA cameras

Data rates of up to 130 megabytes per second

Allows remote location of camera, up to 10 kilometers from host computer

Provides electrical isolation between camera and host





RCX C-Link

Features

Attaches directly to the MDR-26 connector at the back of the camera (no Camera Link cables required)

Sends data to an EDT PCI DV FOX frame grabber

Two RCX C-Link modules can be used to form a fiber optic extension cord

Long range, up to 300 meters standard at 1.25 gigabaud, 10 kilometers with extended range option

Electrically isolates camera from computer

Data rates approaching 250 megabytes per second when operating at 2.5 gigabaud; can approach 750 megabytes per second in full-mode configuration

Description

The EDT RCX C-Link is a fiber optic adapter for Camera Link cameras. It is similar to the EDT RCX module, a fiber optic adapter for use with parallel differential cameras.

The EDT RCX C-Link attaches directly to the back of the camera, taking little more room than a Camera Link cable connector. An LC duplex fiber optic cable plugs into the RCX C-Link to allow communication with a PCI DV FOX fiber optic frame grabber board. EDT software drivers provide the same programmer interface to the PCI DV FOX as to the standard PCI DV C-Link board.

Cameras operating in Camera Link medium- or full-mode have two connectors on the back, so two separate RCX C-Link modules are required. Each RCX C-Link communicates with one of the ports of a PCI DV FOX frame grabber. (Full mode with the PCI DV FOX frame grabber is of limited use due to its 200 megabytes per second limitation.)

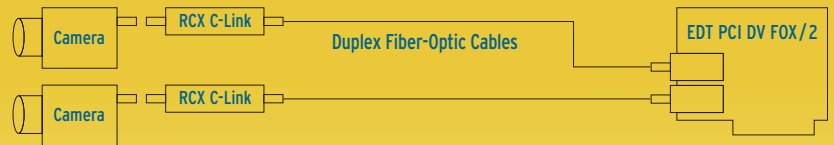
Two RCX C-Link modules may be used to form a fiber optic extension cord, with one module at the camera and the other module at the frame grabber. A medium- or full-mode extension cord uses additional RCX C-Link pairs.

The block diagrams show some of the ways the RCX C-Link (and PCI DV FOX) can be configured. These are only a few examples; many more combinations are possible.

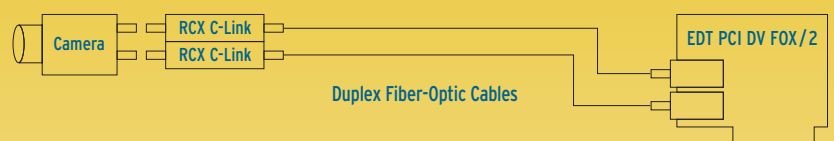
Specifications

Compliance Info	Bit Rate Over Fiber Maximum Data Bandwidth Over Fiber	1.25 and 2.5 GBaud, field selectable Approximately 250 megabytes per second (PCI DV FOX limited to 200 megabytes per second over PCI bus)
	Range	100 meters to 10 kilometers or more. Varies with fiber used, 1.25 vs. 2.5 GBaud selection, number of fiber optic interconnects, which transceiver is stuffed.
	Optical Power Budget	Standard 850 nm transceiver minimum launched power is -10 dBm, receiver sensitivity is -15 dBm maximum, so can lose a maximum of 5 dB in the fiber.
	Camera Link Pixel Clock Ranges Power	20 to 60 MHz, 60 to 80 MHz (field selectable) 4.75 to 18 V DC, 3 watts max
	Fiber Optic Connector Type	LC duplex
	Wavelength Used Over Fiber	850 nm (1300 nm extended range option available)
	Laser Safety	Class 1
	Camera Link Connector	3M MDR-26 plug, entire RCX C-Link module mounts directly to camera
	Camera Link Mode	Base mode uses one RCX C-Link module at the camera end. Medium- and full-mode require additional modules.
	Indicator	One LED, shows the state of the fiber optic link
Physical	Dimensions	1.575" x 0.75" x 2.33" (the LC fiber needs an additional 2.2" beyond the RCX box for a 90° bend)
	Weight	4 oz.
Environmental	Temperature	Operating: 0° to 40°C Non-operating: -20° to 60°C
	Humidity	Operating: 20% to 80% non-condensing @ 40°C Non-operating: 95% non-condensing @ 40°C
Fiber-Optic Cables and Transceivers	Not included; 62.5/125 micron MMF for standard 850 nm transceiver is recommended (use 8/125 micron SMF with 1300 nm extended and Transceivers range option). Both use LC duplex transceivers.	
Power Supply for RCX C-Link	Dimensions	2.4" x 4.5" x 1.5"
	Weight	10 oz.
	Voltage In	100-240 V, 50-60 Hz from AC mains
	Voltage Out	5V DC, 1A
	Connector Used on Power Supply Cable	Switchcraft 760 K (option for Latching 7-pin, Lemo FGG.OB.307.CLAD.56 for auxiliary UART port or other signaling)
Configuration	May be configured in the field for a particular mode of operation. The following configuration choices may be made:	
		Camera pixel clock rate: up to 80 MHz Fiber optic link data rate: 1.25 GBaud or 2.5 GBaud Camera vs. frame grabber end if used as an extension cord
Possible Custom Features	Auxiliary UART port, other custom I/O Other supply voltage ranges Transforms to camera data (e.g., de-interleave, black level adjust) Customer-specified transceivers installed (CWDM or single fiber bidirectional)	

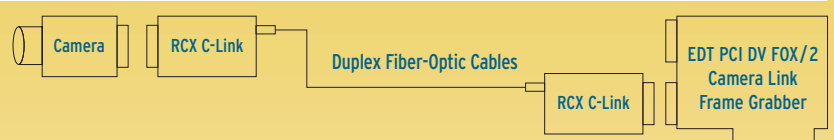
Single or Multiple Base-Mode Camera Link to PCI DV FOX Fiber Optic Frame Grabber



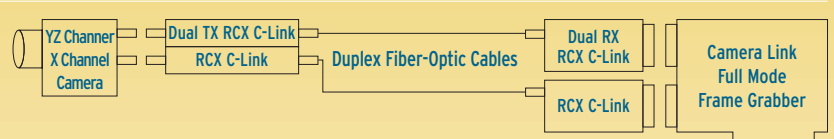
Medium-Mode Camera Link to Fiber Optic Frame Grabber



Base-Mode Camera Link with RCX C-Link Pair Extension Cord



Full-Mode Camera Link to Fiber Optic Frame Grabber





PCI DV FOX + RCX/RCX C-Link

Features

Interfaces digital video cameras to PCI local bus through fiber optic connections

Allows remote location of camera, up to 10 km from host computer

Provides electrical isolation of the camera from the host computer

Single PCI local bus slot supports up to four cameras simultaneously

Supports 8-to 16-bit color or monochrome and 24-bit RGB resolution

Aggregate data rates to 200 megabytes per second sustained as supported by the host

Four-channel DMA to host main memory

Programmable mode, exposure time, and triggering

Remote modules available for Camera Link, LVDS, and RS-422

Description

The PCI DV FOX is EDT's second-generation fiber optic interface for use with digital cameras. One to four cameras can be remotely located up to 10 km with the extended range option. The PCI DV FOX occupies one PCI slot of the host computer. Each camera must have its own fiber optic interface through which it can communicate with the PCI DV FOX in the host computer. An EDT RCX module converts the Camera Link or LVDS/RS-422 signals from most digital cameras to fiber optic cable. Alternately, this fiber optic interface may be incorporated in the camera. Contact EDT for more information.

The PCI DV FOX contains a field-programmable gate array. This gate array can be updated from the host computer to accommodate new camera types.

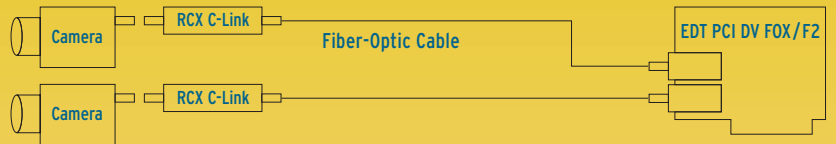
The block diagrams show the PCI DV FOX being used with the RCX C-Link module in example configurations. These are only a few examples; many more combinations are possible.

Two RCX modules can be used as a fiber optic extension cord to EDT or other frame grabbers. In this configuration, digital camera data submitted to one RCX module is replicated at the output of a second module. See the specific data sheets for more details.

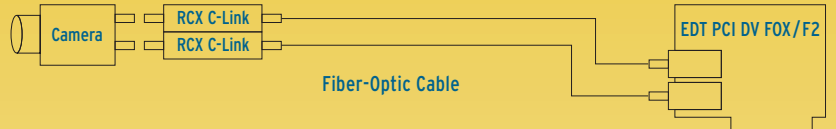
Specifications

Video Interface	The separate RCX modules from EDT interface to AIA digital cameras of up to 24 data bits through an AMP 787169-7 high density 68-pin connector* (RS-422 and LVDS modules) or an MDR 26-pin connector (RCX C-Link). *Manufactured by AMP Inc. 1-800-522-6752 EDT manufactures cables for a wide variety of cameras. For a complete list, see our Digital Video cable list.	
PCI Board	Single PCI local bus slot PCI 2.1s 6 MHz (can operate in 133 MHz PCI-X slot or standard 33 MHz PCI slot) 32 bits (can operate in 32-or 64-bit slot)	
Physical	Dimensions	3.8" x 5.05"
	Weight	3.3 oz.
Power	3 Amp at 3.3 V from host computer PCI bus	
Environmental	Temperature	Operating: 10° to 40°C Non-operating: -20° to 60°C
	Humidity	Operating: 20% to 80% non-condensing @ 40°C Non-operating: 95% non-condensing @ 40°C
RCX Module (Camera Link)	See the separate data sheet for specifications on the RCX C-Link module.	
RCX Module (LVDS and RS422)	See the separate data sheet for specifications on the LVDS and RS-422 modules.	
Laser Safety	Class 1	
Fiber-Optic Cables and Transceivers	When ordering, choose either the 850 nm transceiver for low cost or the 1300 nm transceiver for long distances, with LC connectors. and Transceivers Fiber optic cables are not included in the PCI DV FOX as shipped. See our cable list for optional fiber optic cables available from EDT.	
850 nm VCSEL Transceiver	Fiber Type 62.5/125 mm MMF	Distance 300 m
1300 nm Laser Transceiver	Fiber Type 8/125 mm MMF 62.5/125 mm MMF	Distance 10 km 300 m

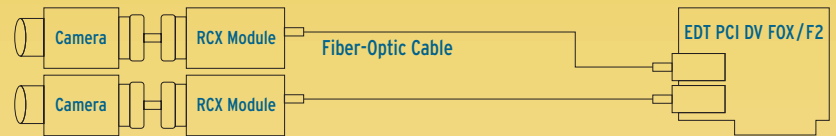
Single or Multiple Base-Mode Camera Link to PCI DV FOX Fiber Optic Frame Grabber



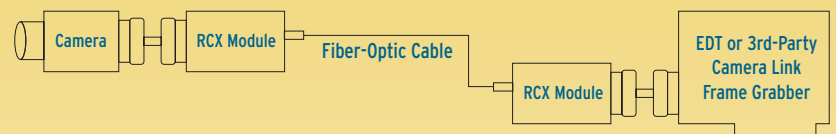
Medium-Mode Camera Link to Fiber Optic Frame Grabber



Single or Multiple LVDS or RS422 Cameras with RCX to PCI DV FOX Fiber Optic Frame Grabber



Single LVDS or RS422 Cameras with RCX Pair Extension Cord





PCI DV C-Link

Description

The PCI DV C-Link provides high-resolution image capture for Camera Link monochrome and color digital cameras. Two MDR-26 pin connectors (Camera Link standard) are provided, for two base-mode or one medium-mode Camera Link camera.

The PCI DV C-Link is a dual-channel DMA interface with 220 megabytes per second capability in a 66 MHz slot or 117 megabytes per second in a 33 MHz slot. Spatial and depth resolution and the number of buffers are limited only by the host memory. Maximum camera speed is determined by the bandwidth available on the host PCI bus. Images can be captured and displayed in real time. The compact, half-length board fits in any PCI slot.

Included with the board are drivers for all supported operating systems, SDK including C language libraries, utilities, examples, camera configuration files, Camera Link standard DLL for camera control, and image capture/display GUI.

Specifications

Video Interface	A field-programmable gate array is configured for a specific camera or class of cameras from a PROM at boot time, and registers defining specific camera behavior are set when the driver is loaded. Thirty-two LVDS signals are configured as inputs or outputs, as required by the camera. The PCI DV C-Link does not include frame buffer memory. Video data is stored in host memory as required by the camera and application.	
cPCI Compliance	P1386.1	
PCI Bus Compliance	PCI Version	PCI 2.3
	Data Width	32 bits
	Number of Slots	1
	DMA	Yes
	PCI Bus Memory Space	Approximately 66 KB
	Clock Rate	33 MHz or 66 MHz
Device Interface	4 KB FIFO for input Onboard UART for Camera Link Serial	
Cables	Standard 3M Camera Link cables (3M P/N 14X26-SZLB-XXX-OLC). Cable assemblies are typically provided with the camera. Cables and connectors are available from 3M.	
Physical	Dimensions	5.0" x 3.6" x 0.5"
	Weight	2.8 oz.
	Connectors	Two MDR-26 pin connectors
Power	1 amp @ 3.3V DC	
Environmental	Temperature	Operating: 10° to 40°C Non-operating: -20° to 60°C Operating (extended temp): -40° to 85°C
	Humidity	Operating: 20% to 80% non-condensing @ 40°C Non-operating: 95% non-condensing @ 40°C
Noise	0 dB	
Mean Time Between Failures	Estimated at 200,000 hours	

Features

Single PCI local bus slot

Up to 28 bits per channel

Direct memory access to host memory; camera resolution independent

On-board region of interest control

PCI local bus data rates up to 220 megabytes per second or maximum supported by host

Can support one or two base-mode, or one medium-mode camera

Triggering via internal trigger, external trigger, programmable pulse-width, or free run

Lower-cost single-connector version also available (base mode only)

Also available in the PMC and Compact PCI form factor

Description

The PCI DVa provides high-resolution image capture for digital video cameras. A wide variety of cables can be used, because the PCI DVa uses one 80-pin connector. Spatial and depth resolution and the number of buffers are limited only by the host memory. Images can be captured and displayed in real time. Support for most camera models is available.

The PCI DVa is similar to EDT's PCI DV; however, the PCI DVa can run at 66 MHz when installed in a 66 MHz slot, yielding higher speeds. Speeds of 210 megabytes per second have been measured with the PCI DVa using a high performance host versus 93 megabytes per second with the PCI DV.



PCI DVa

Specifications

Video Interface	A field-programmable gate array is configured for a specific video camera when the driver is loaded. Thirty-six LVDS or RS-422 signals are configured as inputs or outputs, as required by the camera. Outputs can also be configured as single-ended for TTL camera control lines. The PCI DVa does not include frame buffer memory. Video data is stored in host memory as required by the camera and application.	
PCI Bus Compliance	PCI Version Data Width Number of Slots DMA PCI Bus Memory Space Clock Rate	PCI 2.3 32 bits 1 Yes Approximately 66 KB 33 MHz or 66 MHz
Cables	Cables to connect the PCI DVa to a variety of cameras are available. For part numbers, refer to our PCI DV cable list. Cables are typically 10 feet long unless otherwise specified. Longer cables can be special ordered.	
Physical	Dimensions Weight Connector	5.01" w x 4.20" h 3.3 oz. AMP 787190-8 high-density 80-pin (mates with AMP 749621-8, backshell 749196-2)
Power	Less than 0.2 Amp, 3 V	
User Interface Xilinx	S200E or optional S600E	
Environmental	Temperature Humidity	Operating: 10° to 40°C Non-operating: -20° to 60°C Operating (extended temp): -40° to 85°C Operating: 20% to 80% non-condensing @ 40°C Non-operating: 95% non-condensing @ 40°C
Noise	0 dB	
Mean Time Between Failures	150,000 hours	

Features

Single PCI local bus slot

Supports 8-through 24-bit resolution

Direct memory access to host memory; camera resolution independent

33 or 66 MHz, 3 or 5V PCI capable

32-bit PCI; also works in 64-bit slot

Data rates up to 210 megabytes per second, as supported by host

Programmable mode, exposure time, gain black level, and triggering

Supports AIA serial command interface over RS-422 and RS-232 serial lines



PMC DV C-Link

Description

The PMC DV C-LINK provides high-resolution image capture for Camera Link monochrome and color digital cameras. One MDR-26 pin connector (Camera Link standard) is provided, which supports one base-mode Camera Link camera.

The PCI DV C-Link is a dual-channel DMA interface with 220 megabytes per second capability in a 66 MHz slot, or 117 megabytes per second in a 33 MHz slot. Spatial and depth resolution and the number of buffers are limited only by the host memory. Images can be captured and displayed in real time. The board complies with PMC form factor specifications and will fit in any PMC slot.

Specifications

Video Interface	A field-programmable gate array is configured for a specific camera or class of cameras from a PROM at boot time, and registers defining specific camera behavior are set when the driver is loaded. Thirty-two LVDS signals are configured as inputs or outputs, as required by the camera. The PMCDV C-Link does not include frame buffer memory. Video data is stored in host memory as required by the camera and application.	
PMC Compliance	P1386.1	
PCI Bus Compliance	PCI Version	PCI 2.3
	Data Width	32 bits
	Number of Slots	1
	DMA	Yes
	PCI Bus Memory Space	Approximately 66 KB
	Clock Rate	33 MHz or 66 MHz
Cables	Standard 3M Camera Link cables (3M P/N 14X26-SZLB-XXX-OLC). Cable assemblies are typically provided with the camera. Cables and connectors are available from 3M.	
Physical	Dimensions	74mm x 152mm
	Weight	2.8 oz.
	Connectors	One MDR 26-pin connector
Power	1 amp at 3.3V DC	
Environmental	Temperature	Operating: 10° to 40°C Non-operating: -20° to 60°C Operating (extended temp): -40° to 85°C Non-operating: -40° to 90°C
	Humidity	Operating: 20% to 80% non-condensing @ 40°C Non-operating: 95% non-condensing @ 40°C
Noise	0 dB	
Mean Time Between Failures	Estimated at 200,000 hours	

Features

Single PMC slot

Up to 28 bits per channel

Direct memory access to host memory; camera resolution independent

66 MHz, 32-bit PCI board

PCI local bus data rates up to 220 megabytes per second or maximum supported by host

Can support one base-mode Camera Link camera

Also available in the PCI and C ompact PCI form factor

Description

The cPCI DV C-Link provides high-resolution image capture for Camera Link monochrome and color digital cameras. Two MDR 26-pin connectors (Camera Link standard) are provided, which support one or two base-mode Camera Link cameras or one medium-mode camera.

The cPCI DV C-Link is a dual-channel DMA interface with up to 220 megabytes per second capability (200 MB observed) in a 66 MHz slot, or 117 megabytes per second (90 megabytes observed) in a 33 MHz slot. Spatial and depth resolution and the number of buffers are limited only by the host memory. Images can be captured and displayed in real time. The board complies with Compact PCI form factor specifications and will fit in any cPCI slot.



cPCI DV C-Link

Specifications

Video Interface	A field-programmable gate array is configured for a specific camera or class of cameras from a PROM at boot time, and registers defining specific camera behavior are set when the driver is loaded. Thirty-two LVDS signals are configured as inputs or outputs, as required by the camera. The cPCI DV C-Link does not include frame buffer memory. Video data is stored in host memory as required by the camera and application.	
cPCI Compliance	P1386.1	
PCI Bus Compliance	PCI Version	PCI 2.3
	Data Width	32 bits
	Number of Slots	1
	DMA	Yes
	PCI Bus Memory Space	Approximately 66 KB
	Clock Rate	33 MHz or 66 MHz
Device Interface	4 KB FIFO for input Onboard UART for Camera Link Serial	
Cables	Standard 3M Camera Link cables (3M P/N 14X26-SZLB-XXX-0LC). Cable assemblies are typically provided with the camera. Cables and connectors are available from 3M.	
Physical	Dimensions (not including back panel/connectors)	9.2" x 6.3" x 0.4"
	Weight	9.4 oz.
	Connectors	Two MDR-26 pin connectors One DB-9 pin connector (diagnostic)
Power	1 amp at 3.3V DC	
Environmental	Temperature	Operating: 10° to 40°C Non-operating: -20° to 60°C Operating (extended temp): -40° to 85°C
	Humidity	Operating: 20% to 80% non-condensing @ 40°C Non-operating: 95% non-condensing @ 40°C
Noise	0 dB	
Mean Time Between Failures	Estimated at 200,000 hours	

Features

Occupies one 6U or 3U Compact PCI Slot

Up to 28 bits per channel

Direct memory access to host memory; camera resolution independent

PCI local bus data rates up to 220 megabytes per second or maximum supported by host

66 MHz, 32-bit PCI board

Can support one or two base-mode, or one medium-mode Camera Link camera

Triggering via internal trigger, external trigger, programmable pulse-width, or free run



PMC DV CLS

Description

The PCI DV CLS is a simulator that generates Camera Link camera data. It uses an easily modified text-based configuration script that describes the timing parameters of the camera to be simulated.

Library calls in C allow the user to define appropriate responses to UART commands from the frame grabber.

Known image data allows easy debug of frame grabber application code. The PCI DV CLS allows system debug when target camera is unavailable.

The PCI DV CLS does not include frame buffer memory; image data is stored in host memory as required by the application.

Specifications

PCI Local Bus Compliance	PCI Version Data Width Number of Slots DMA PCI Bus Memory Space Clock Rate External Connectors	PCI 2.3 32 bits 1 Yes Approximately 66 KB 33 MHz or 66 MHz Two MDR-26 Camera Link connectors
Power	Less than 2 amps, 3V	
Environmental	Temperature Humidity	Operating: 0° to 40°C Non-operating: -20° to 60°C Operating: 20% to 80% non-condensing @ 40°C Non-operating: 95% non-condensing @ 40°C
Physical	Dimensions Weight	5.01" x 4.20" 3.3 oz. typical
Noise	0 dB	
Mean Time Between Failures	150,000 hours	

Features

- Simulates Camera Link digital cameras, base-mode and 32-bit medium mode
- Single PCI local bus slot
- Direct Memory Access (DMA) from host memory for image data
- DMA data rates up to 200 megabytes per second, as supported by host
- Internal counters may be chosen as alternate source of image data
- Supports triggering by line or frame from camera control lines
- Supports Camera Link clock from 20 to 85 MHz in increments of 0.250 MHz
- Allows emulation of camera UART commands
- 33 to 66 MHz, 3 or 5V PCI-capable
- 32-bit PCI, also works in 64-bit slot

Description

The PCI CDa board provides one high-speed 16-bit parallel channel or an optional 16 synchronous serial channels between an external device and a PCI local bus computer (16 synchronous serial channels*). The device interface uses LVDS- or RS-422-compatible driver/receivers connected to a field-programmable gate array (FPGA).

The PCI CDa uses direct memory access (DMA) and asynchronous I/O to achieve transfer rates to or from memory of up to 210 megabytes per second (observed). The hardware protocol is synchronous; in other words, all data and control signals are sampled with a clock transmitted along with the data and control signals. This clock may be generated by the DMA interface or the user device or both. All signals are differential using LVDS (or optional RS-422) specifications. The PCI CDa includes a versatile, straightforward protocol but optional customer-specific protocols may be developed.

Both 16-bit parallel and 16 synchronous serial channels are 100 percent VHDL in the user interface Xilinx FPGA. EDT allows access to the source VHDL for custom designs.

*For 16-channel capability, the CDa must have an optional Xilinx XC2S600e installed and use the `ssd16io` configuration file.

Features

Transfer rate up to 210 megabytes per second (single channel), 70 megabits per second per channel (16 channels)

Integrated FIFOs

Implements a high-speed DMA channel between an external device and PCI local bus computer

RS-422 or LVDS (EIA644) driver/receivers

33 or 66 MHz clock speed, 3 or 5V PCI-capable

16-bit parallel or 16-channel synchronous serial

32-bit PCI; also works in a 64-bit slot

User-programmable FPGA Xilinx XC2S100E or XC2S600E

Synchronous protocol

Single PCI local bus slot



PCI CDa

Specifications

PCI Bus Compliance	PCI Version	PCI 2.2
	Data Width	32 bits
	Transfer Size	16-bit parallel: up to 1024 bytes per transfer 16-channel synchronous serial: 64 bytes per transfer
	DMA	Yes
	PCI Local Bus Memory Space	Approximately 66 KB
	Clock Rate	33 MHz or 66 MHz
External Connectors	AMP 787190-8 high-density 80-pin (mates with AMP 749621-8, backshell 749196-2)	
Buffers	Integrated FIFOs for input and output	
Protocol	16-bit parallel: synchronous streaming 16-channel: synchronous serial	
User Interface Xilinx	XC2S100E or XC2S600E (required for 16-channel synchronous serial)	
Clock Generators	1 PLL clock generator	
Physical	Number of Slots	1
	Dimensions	5.01" w x 4.20" h
	Weight	3.3 oz.
Power	3 or 5 V	
	Uses less than 2 amps at 3V	
Environmental	Temperature	Operating: 10° to 40°C Non-operating: -40° to 70°C
	Humidity	Operating: 1% to 90% non-condensing @ 40°C Non-operating: 95% non-condensing @ 40°C



PCI 53B

Description

The PCI 53B provides a complete single slot MIL-STD 1553B interface for PCI bus computers. The 1553B interface is a 1 Mbit per second serial bus interface, used where reliability in extreme environments is essential. After initialization the application program can configure the card as required.

The PCI 53B uses an onboard SPARC processor and can be reprogrammed for any 1553 protocol. The PCI 53B supports the full 1553B standard but may be configured to detect any standard command or sub-command as illegal.

Specifications

PCI Local Bus Compliance	PCI Version Data Width Number of Slots Clock Rate	PCI 2.1s 32 bits 1 33 MHz or 66 MHz
Physical	Dimensions Weight	7.0" x 4.2" x 0.5" 6 oz.
Interface	Primary and secondary 1553 interface	King 1994-1-9 Triax connector
Controls	User programmable register selects Direct or Transformer-coupled	
Environmental	Temperature Humidity	Operating: 10° to 40°C Non-operating: -20° to 60°C Operating: 1% to 90% non-condensing @ 40°C Non-operating: 95% non-condensing @ 40°C
Memory	Flash ROM DRAM	512 KB 16 MB
Power	3.3 or 5V at 2 amp, +12 V 0.05 amp, -12 V 0.05 amp	

Features

Supports minimum 4 microsecond intermessage gap and RT response

Single PCI Bus slot

Powerful real-time bus controller scheduling capabilities on board

Simultaneously acts as single or multiple Remote Terminal, Bus Controller, and Bus Monitor

Supports all mode codes for dual redundant operation

Error insertion and detection capabilities

Extensive built-in test facility including continuous monitoring of transmitted data



**לפרטים פנה למילטרם
הנציגה הבלעדית בישראל
בטלפון: 09-9581860**

שלוחה 110 (רפי) • שלוחה 122 (שגיא)
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דוא"ל: rafit@miltram.com

סמינר מודיעין טקטי

תקשורת ומיחשוב

הסמינר יתקיים ביום ג',
6 בפברואר 2007, בשעה 9:00,
במלון דן-אכדיה, הרצליה

מקלטים צרי סרט בתדרים 50KHz-3GHz
מקלטים רחבי סרט בתדרים 50KHz-3GHz
מקלטי ELINT בתדרים 0.5GHz-18-22GHz
מערכות אנליזה לספקטרום התדרים
תקשורת סיבים אופטיים
תקשורת לוויינים
מיחשוב נייד מוקשח

גזור ושלח **סמינר מודיעין טקטי**

שם פרטי _____ שם משפחה _____
מפעל _____ מחלקה _____
כתובת _____
טלפון _____ פקס _____ דוא"ל _____

נא אשרו השתתפותכם בסמינר בפקס: 09-9574383
או בדוא"ל: militram@militram.com